WHIRLBOB, the Whirlpool based Variant of STRIBOB

Lighter, Faster, and Constant Time

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Abstract. WHIRLBOB, also known as STRIBOBr2, is an AEAD (Authenticated Encryption with Associated Data) algorithm derived from STRIBOBr1 and the Whirlpool hash algorithm. WHIRLBOB/STRIBOBr2 is a second round candidate in the CAESAR competition. As with STRIBOBr1, the reduced-size Sponge design has a strong provable security link with a standardized hash algorithm. The new design utilizes only the LPS or ρ component of Whirlpool in flexibly domain-separated BLNK Sponge mode. The number of rounds is increased from 10 to 12 as a countermeasure against Rebound Distinguishing attacks. The 8×8 - bit S-Box used by Whirlpool and WHIRLBOB is constructed from 4×4 - bit "MiniBoxes". We report on fast constant-time Intel SSSE3 and ARM NEON SIMD WHIRLBOB implementations that keep full miniboxes in registers and access them via SIMD shuffles. This is an efficient countermeasure against AES-style cache timing side-channel attacks. Another main advantage of WHIRLBOB over STRIBOBr1 (and most other AEADs) is its greatly reduced implementation footprint on lightweight platforms. On many lower-end microcontrollers the total software footprint of π+BLNK = WHIRLBOB AEAD is less than half a kilobyte. We also report an FPGA implementation that requires 4,946 logic units for a single round of WHIRLBOB, which compares favorably to 7,972 required for Keccak / Keyak on the same target platform. The relatively small S-Box gate count also enables efficient 64-bit bitsliced straight-line implementations. We finally present some discussion and analysis on the relationships between WHIRLBOB, Whirlpool, the Russian GOST Streebog hash, and the recent draft Russian Encryption Standard Kuznyechik.

Keywords: WHIRLBOB, STRIBOBr1, Authenticated Encryption, Sponge Designs, Timing Attacks, Whirlpool, Streebog, CAESAR Competition.

1 Introduction

STRIBOBr2, or WHIRLBOB, is an Authenticated Encryption with Associated Data (AEAD) algorithm and a CAESAR ("Competition for Authenticated Encryption: Security, Applicability, and Robustness") [21] competition Second Round Candidate [58].

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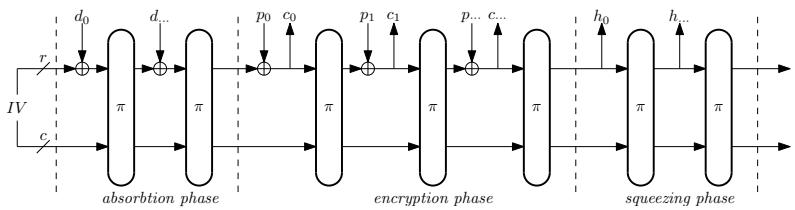

Fig. 1. A simplified view of a Sponge-based AEAD. Padded Secret Key, Nonce, and Associated Authenticated Data - all represented by d_u words - are first "absorbed" into the state. The π permutation is then also used to encrypt data p_i into ciphertext c_i (or vice versa) and finally to "squeeze" out a Message Authentication Code h_i.

AEAD algorithms and modes such as GCM [45] provide both confidentiality and integrity protection for messages in a single step, thus eliminating the need for a separate MAC algorithm such as HMAC [46]. This has clear advantages for performance and implementation footprint.

WHIRLBOB uses STRIBOBr1's BLNK Sponge AEAD mode and parameters without modification. Outside the CAESAR context, BLNK can be also used in a wider set of applications, even to build entire secure lightweight protocol suites [55]. A sponge mode requires only a single cryptographic component; an unkeyed cryptographic permutation π (See Figure 1). As with other provable Sponge modes, we assume that π is indistinguishable from a random permutation. This work focuses on π permutation design and implementation – for BLNK padding details and analysis we refer to [32,54,56,57].

The STRIBOBr1 CAESAR [56] candidate was derived from the Russian GOST hash standard Streebog [26]. In close examination Streebog appears to be modeled after the Whirlpool hash [4], with substantial modifications. However, STRIBOBr1 and WHIRLBOB only differ in the particular numerical selections for tables C, S, and L. These components, $L \circ P \circ S$ or the "LPS permutation" is derived directly from that of Whirlpool for WHIRLBOB. The program code of 64-bit reference implementations is essentially equivalent for both algorithms. Both STRIBOBr1 and WHIRLBOB have 12 rounds.

We show that the particular structure of the Whirlpool components allows WHIRLBOB to have much more efficient SIMD, constant-time, lightweight, and hardware implementations. One of our aims is to allow the same implementation core (such as a special instruction or coprocessor of a SoC [56]) to be also used for unkeyed hashing according to the Whirlpool standard. This is useful in applications that also require efficient standards-compliant certificate signature processing.

The corresponding standardized, Miyagushi-Preneel hash functions Streebog and Whirlpool require two (or more) times as much as state and processes data in bigger chunks when compared to STRIBOBr1 and WHIRLBOB. Our BLNK Sponge mode also supports randomized hashing and MACing without encryption. Our Sponge variants are slightly faster than the original hashes, yet have a provable security relation. All security parameters remain unmodified from STRIBOBr1.

2 WHIRLBOB

As with STRIBOBr1, the state consists of $b = 512$ bits, split in our BLNK mode as:

$r = 256$ - bit *rate* "block size", which directly interacts with output and input.
$c \approx 254$ - bit *capacity*, which is the secret state. Some bits are lost to padding.

These two halves are mixed together by a keyless, random-indistinguishable permutation π. According to theorems such as those given in [32,56] this is sufficient for $k = 192$ - bit secret key security level when less than 2^{64} bits are processed under same key and nonce pair. For the CAESAR variant the nonce length is fixed at $n = 128$ bits.

Despite having almost equivalent speed and size on generic 64-bit platforms, the size and performance characteristics of STRIBOBr1 and WHIRLBOB differ significantly on various implementation platforms such as FPGA, low-end microcontrollers, SIMD systems, and in bitslicing implementations.

WHIRLBOB's permutation π is indeed highly similar to AES. In case of STRIBOBr1, the "Russian 512-bit block AES" permutation had to be somewhat laboriously uncovered from the structure (see Section 5.3), but the particularities and history of Whirlpool make the connection immediately clear.

2.1 Structure of the π Permutation

The computation of π follows almost exactly the operation of the internal key schedule of Whirlpool 3.0 [4]. The only modification is that the number of rounds is increased from $R = 10$ to $R = 12$ for extra security margin against Rebound Distinguisher attacks [35,36]. [3]

To compute $\pi(x_0) = x_{12}$ we iterate the $\mathsf{LPS} = L \circ P \circ S$ composite mixing function with round constants C_r. For rounds $0 \leq r < 12$:

$$x_{r+1} = L(P(S(x_r))) \oplus C_r. \tag{1}$$

If we use the AES-style notation of Whirlpool, S is equivalent to `SubBytes`, P corresponds to `ShiftColumns`, L to `MixRows`, followed by `AddRoundKey`.

We write the 512-bit state as a matrix $M[\,0 \cdots 7\,][\,0 \cdots 7\,]$ of 8×8 bytes, which can be serialized to a byte vector as $\texttt{vec}[\,8i + j\,] = M[\,i\,][\,j\,]$.

S: `SubBytes`: Each one of the 64 bytes in the state is substituted using the (singular) 8×8 - bit S-Box described in Section 2.2. For $0 \leq i, j < 8$

$$M'[\,i\,][\,j\,] \leftarrow S(M[\,i\,][\,j\,]). \tag{2}$$

P: `ShiftColumns`: A byte shuffle. For $0 \leq i, j < 8$

$$M'[\,(\,i + j\,) \bmod 8\,][\,j\,] \leftarrow M[\,i\,][\,j\,]. \tag{3}$$

[3] These attacks would not be directly applicable with the BLNK mode anyway. This is because the attacker can never access more than r bits of the internal state.

$\underline{L}$: `MixRows`: Each of the 8 row vectors

$$V_i = (M[\,i\,][\,0\,], M[\,i\,][\,1\,], \cdots M[\,i\,][\,7\,]) \tag{4}$$

is individually multiplied by a circulant, low-weight 8×8 MDS matrix in the finite field $\mathsf{GF}(2^8)$ characterized by primitive polynomial $p(x) = x^8 + x^4 + x^3 + x^2 + 1$.

$$V_i' = V_i \cdot \begin{pmatrix} \texttt{01 01 04 01 08 05 02 09} \\ \texttt{09 01 01 04 01 08 05 02} \\ \texttt{02 09 01 01 04 01 08 05} \\ \texttt{05 02 09 01 01 04 01 08} \\ \texttt{08 05 02 09 01 01 04 01} \\ \texttt{01 08 05 02 09 01 01 04} \\ \texttt{04 01 08 05 02 09 01 01} \\ \texttt{01 04 01 08 05 02 09 01} \end{pmatrix}. \tag{5}$$

$\underline{C_r}$: `AddRoundKey`: The key schedule operation is effectively equivalent to the one used by Whirlpool's "internal block cipher" W. Blocks of eight bytes from the S-Box are used round keys C_r for the first row. For round $0 \leq r < 12, 0 \leq j < 8$:

$$M'[\,0\,][\,j\,] \leftarrow M[\,0\,][\,j\,] \oplus S(\,8r + j\,) \tag{6}$$

Rest of the rows are unaffected by C_r. For $1 \leq i < 8, 0 \leq j < 8$:

$$M'[\,i\,][\,j\,] \leftarrow M[\,i\,][\,j\,]. \tag{7}$$

We offer the listing of Appendix A as WHIRLBOB v1.0 π reference implementation. Whirlpool ISO Standard trace test vectors can be used to verify the correctness of this π implementation up to $r = 10$ [30]. One simply observes the keying "line" of these traces and ignores the encryption "line".

2.2 The S-Box

The Whirlpool and WHIRLBOB 8×8-bit S-Box design utilizes three 4×4 - bit "mini-boxes" given in Table 1: E, E^{-1}, and R. Figure 2 shows how these are used to construct the 8×8 - bit S-Box.

This computation can even be performed on the fly on 4-bit microcontrollers. FPGA implementations save a significant number of LUTs by explicitly utilizing the 4-bit structure rather than implementing a general 8×8 lookup table. These small S-Boxes can often fit into SIMD registers and accessed via constant-time shifts or shuffles, thus enabling implementations resistant to timing attacks.

2.3 BLNK Mode

The padding details and operation of BLNK Sponge mode for WHIRLBOB and STRIBOBr1 are equivalent. Please see [58] for details. The mode is based derived from the Blinker light-weight protocol [53], but limited to CAESAR use case.

Table 1. Three 4×4 miniboxes that are used to build the 8×8 S-Box in Whirlpool 3.0 and WHIRLBOB 1.0.

x	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
$E(x)$	1	B	9	C	D	6	F	3	E	8	7	4	A	2	5	0
$E^{-1}(x)$	F	0	D	7	B	E	5	A	9	2	C	1	3	4	8	6
$R(x)$	7	C	B	D	E	4	9	F	6	3	8	A	2	5	1	0

3 Implementation

The entire byte-oriented implementation of π fits onto a single page; See Appendix A. Remarkably, in addition to π, only the S-Box `wbob_sbox[256]` (See Section 2.2) together with minimal BLNK logic are required for full AEAD implementation. On many microcontrollers WHIRLBOB's entire software footprint is in the 500B range. Slightly more is required for a shared secret handshake protocol and two-way secure BLINKER protocol [55].

This is a significant improvement over STRIBOBr1, which typically needs almost 2kB. STRIBOBr1 is also much slower and larger on low-end microcontrollers due to the "heavy" MDS matrix. The reference implementation is written for compactness and clarity; it is not optimal when it comes to speed or size. We refer to section 7.3 of [4] for techniques that greatly reduce the number of XORs required, resulting in increased processing speed. Additional tables will be required, however, and this will increase the overall implementation size.

3.1 Constant-Time SIMD Implementation

Due largely to Whirlpool's S-Box structure and generous parallelism, it is well suited for high speed, constant-time implementation on Single Instruction Multiple Data (SIMD) architectures. Here we focus on ARM's NEON as the reference architecture since the state layout fits the registers nicely, but also consider Intel's SSSE3 as another explicit example. The goal is to improve performance, while at the same time avoiding memory-resident table lookups that cause execution time to depend on the data cache state and thus algorithm state (the crux of cache timing attacks).

Related work in this area includes simulated ISA extensions to a RISC architecture for parallel table lookups to speed up Whirlpool [28]. These extensions are then used to build essentially a hardware-assisted analogue of the traditional T tables software implementation – storing the state in rows and issuing a single instruction to perform 8 parallel lookups from the 8-bit S-Box input to the 64-bit linear layer output and XOR-summing the results, repeated for each row. AES [27] and Anubis [18] can also take advantage of SSSE3's variable byte shuffle instruction for fast and secure implementations.

NEON has 32×64 - bit SIMD registers and SSSE3 16×128 - bit. We store the state column-wise (one column per NEON register, two columns per SSSE3 register), i.e. byte position j of register i contains the state byte in column i and row j. The `SubBytes` step is not sensitive to this ordering, but both `ShiftColumns` and

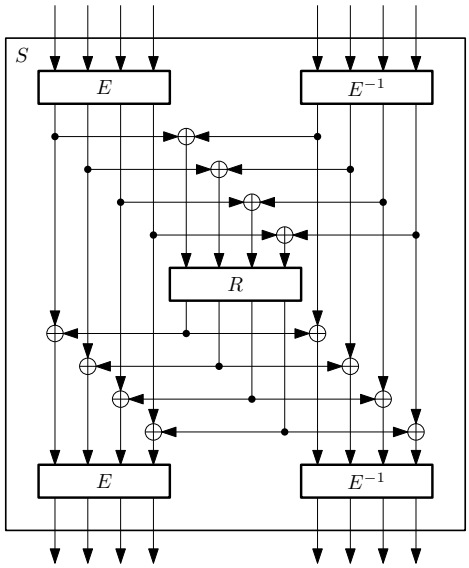

Fig. 2. The WHIRLBOB 8×8 - bit S-Box is constructed from three 4×4 - bit "miniboxes". In this diagram the most significant bits are on the left: E operates on the higher nybble.

`MixRows` are. Since both of these architectures feature variable byte shuffle instructions (`vtbl.u8` for NEON and `pshufb` for SSSE3), implementing `SubBytes` is a direct translation of Figure 2 to these instructions. This amounts to 40 NEON shuffles and half as many SSSE3 shuffles. For `ShiftColumns`, NEON uses `vext` for byte-wise register rotation and SSSE3 `pshufb` with constant rotation distances since each register holds two columns. For `MixRows` we use the row formula from the Whirlpool specification [4, Sec. 7.3] where the multiplications by x are a simple left shift (native on NEON, integer addition on SSSE3) and conditional XOR (operand masked by signed right shift on NEON, comparison on SSSE3). The formula is fairly symmetric around even and odd byte positions – while NEON implements it as written with 24 multiplications, SSSE3 slightly rearranges a few registers to parallelize across the full 128-bit register width and use half as many multiplications.

3.2 Generic Constant-Time Bitsliced Implementation

The byte-oriented $8 \times 64 = 512$ - bit state can be rapidly split into eight 64-bit registers. The parallelism evident in Figure 2 helps to speed up bitsliced implementation. We see that for 2/3 of the time, the S-Box has effectively two independent 4-bit execution paths. Interleaving these may greatly reduce wait states due to the superscalar architecture employed by most modern CPUs.

Appendix B of the current 2003 Whirlpool specification [4] gives listings with 14-16 instructions/gates for each of the miniboxes (if ANDN instruction is allowed). Those were used in our reference bitsliced implementations.

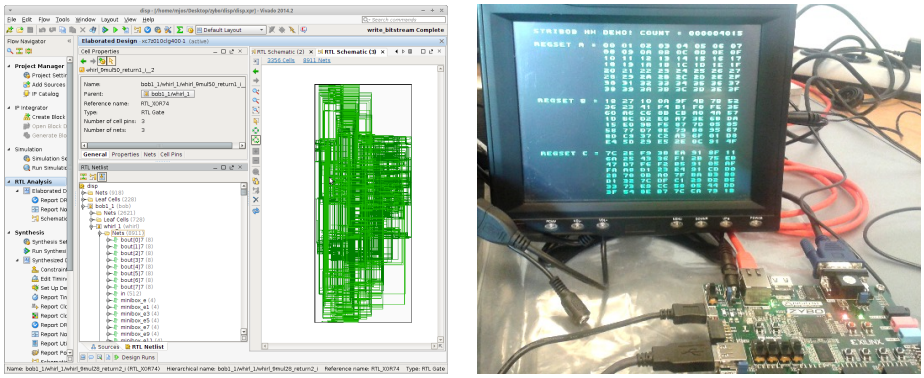

Fig. 3. WHIRLBOB was implemented on the FPGA logic fabric of Xilix Zynq 7010. The implementation integrates with the AXI bus of ARM Cortex A9 on the SoC chip.

3.3 Implementation Summary

We currently have six implementations of WHIRLBOB. They mainly differ in the implementation technique used for the π cryptographic permutation.

- **C 8-bit**: This is the minimal reference implementation which is optimized for clarity and low-resource platforms, corresponding to Appendix A.
- **C 64-bit**: Standard speed-optimized implementation for most platforms, utilizing large lookup tables. Apart from Whirlpool-derived tables, equivalent to the implementation of Sa14E.
- **C Bitsliced**: Straight-line, fully bitsliced implementation without data-dependent branches or lookups. Resistant to timing attacks.
- **NEON Intrinsics**: Fast constant-time version that avoids table lookups by storing 4×4 - bit miniboxes in SIMD registers.
- **SSSE3 Intrinsics**: Similar but for 128-bit SIMD registers.
- **Verilog 12-cycle**: This is the hardware reference implementation. Source code is about 350 lines. Additional logic is required for AXI Bus integration.

Software Implementations. The first three implementations use only C99, and are hence easily portable. See Table 2 for implementation metrics. We also have various embedded implementations. Note that STRIBOBr2 is faster then the (out-of-box, Ubuntu 14.04 LTS) OpenSSL implementation of AES-192 on the same target.
Hardware Implementation. The hardware implementation has been proven on FPGA (Figure 3). The SÆHI proposal reports total post place-and-route utilization on Artix-7 of 4,946 logic units for a single round of WHIRLBOB, which compares favourably to 7,972 required for Keccak/Keyak [56]. Throughput is roughly 2 MB/s for each MHz.

4 Comparison with Other AEAD Schemes

At the time of writing the dominant AEAD scheme is the Galois / Counter Mode (GCM) for the AES block cipher [43,45], which is recommended for use with TLS, SSH and

Table 2. Comparing software implementations of WHIRLBOB π.

Target	**Speed**	**Footprint**		**Source**
	MB/sec	Code	Data	C lines
Single Core of 3.4GHz Core i7-4770				
8-bit C99 Reference	7.772	326	256	97
Bitsliced C99 Reference	49.02	4592	768	345
64-bit C99 Reference	139.2	1942	16512	128
SSSE3 (Constant-Time)	**162.3**	1290	1152	256
OpenSSL 1.0.1f AES-192 CBC	*145.6*			
BeagleBone Black 1.0GHz Cortex-A8				
8-bit C99 Reference	0.828	352	256	97
64-bit C99 Reference	3.343	6524	16512	128
Bitsliced C99 Reference	1.435	15704	768	345
NEON (Constant-Time)	9.208	1528	1072	320

IPSec protocols by NSA as part of "Suite B" [19,29,48,59]. GCM message authentication is based on polynomial evaluation in the finite field $\mathsf{GF}(2^{128})$. The required multiplication can be exceedingly slow on lightweight platforms. An LFSR-style implementation of a 128×128 - bit multiplication will require thousands of cycles on 8-bit targets.

It is often more efficient to use the CCM [44,63] double-mode of operation on lightweight platforms, since implementing a full extra AES operation can be faster than the finite field multiplication operation. CCM and GCM are currently the only two FIPS - standardized authenticated modes. The performance characteristics of AES-CCM AEAD can be expected to be very similar to WHIRLBOB due to their structural similarities and relative data bandwidth:

- WHIRLBOB: 12 rounds with 64 S-Boxes for 256 bits of data.
- AES-192-CCM: 2×12 rounds with 16 S-Boxes for 128 bits of data.

There are additional (patented) AES modes which will be faster on 8-bit platforms – such as AES-OTR [40] and AES-OCB [34], and dozens of others. Virtually all AEAD block cipher modes offer lower levels of integrity protection (2^{64} level even for 128-bit tags) and are not directly usable in wider Sponge applications such as non-randomized hashing.

Currently only unoptimized reference implementations are available for most CAESAR candidates [20], making fair performance comparisons difficult. Furthermore, no other CAESAR candidate is targeted at 192-bit security level (apart from AES modes) and little attention has been paid to 8-bit or hardware implementations.

We note that leading full-featured Sponge candidates, directly SHA3 / Keccak - based Ketje Keyak [12] and [6] have significantly slower reference implementation than STRIBOBr1 and WHIRLBOB (Table 3). WHIRLBOB falls very significantly from candidates such as NORX [3] and MORUS [64], which have been designed specifically with 64-bit targets in mind. Our proposal can claim a more conservative security margin when compared to these candidates, however.

Table 3. Relative performance of some CAESAR candidates on a AMD64 reference system in SUPERCOP testing (smaller number indicates faster speed).

MORUS 1280 - 128 [64]	0.09
NORX 64-4-1 [3]	0.19
ASCON-128n [24]	0.89
WHIRLBOB Intel SSSE3 Constant-Time	**1.00**
WHIRLBOB and STRIBOBr1 64-bit Reference	1.26
Lake Keyak [12]	2.23
Ketje Sr. [6]	4.25
PRIMATES (HANUMAN, GIBBON, APE) [2]	50+

`bench.cr.yp.to/web-impl/amd64-titan0-crypto_aead.html`

5 Security Analysis and Design Notes

For analysis of the round function against classical Differential and Linear cryptanalysis we refer to Whirlpool literature [4]. Two additional rounds increase WHIRLBOB's resistance against best known attacks [35,36].

Most of the security arguments and proofs offered for STRIBOBr1 and BLNK in [56] also apply to the new proposal. These are based on indistinguishably arguments for the π permutation and a simple theorem (Thm. 1, Sec. 3.3. in [56]) that loosely ties the compression function in Miyagushi-Preneel mode [41,51] with the indistinguishably of π. A random-indistinguishable π and appropriate padding rules are sufficient to construct Sponge-based hashes [7], Tree Hashes [11], MACs [10], Authenticated Encryption (AE) algorithms [9], and pseudorandom extractors (SHAKEs, PRFs, and PRNGs) [8,47].

5.1 Side-Channel and Implementation Attacks

Due to the minibox structure, we may load the 4×4 - bit tables in registers and access them via constant-time shuffles on Intel SSSE3 and ARM NEON SIMD targets as noted in Section 3.1. WHIRLBOB is also relatively well suited for bitsliced implementation due to its particular S-Box and MDS design as noted in Section 2.2.

Being unconditional straight-line code without data-dependent table lookups, bitsliced and byte shuffling implementations are effective countermeasures against cache timing attacks, which can be mounted against cryptographic primitives with large tables such as AES [1,5,50,62].

A non-constant-time implementation of the S-Box on Whirlpool, Streebog, or STRIBOBr1 on 64-bit platforms typically requires lookup tables of up to $8 \times 256 \times 8 = 16384$B. Even though this size easily fits into the Level 2 cache of any 64-bit system, one may see that timing attacks are possible as L2 caches are not always shared even between different execution cores within a single CPU unit. This is due to the process switching operation of most 64-bit operating systems.

5.2 Historical Modifications to Whirlpool

Whirlpool has received a significant amount of analysis in the almost 15 years since its original publication. Whirlpool was the only hash function in the final NESSIE portfolio in addition to SHA-2 hashes [42]. Whirlpool has also been standardized by ISO as part of ISO/IEC 10118-3:2004 [30].

The amended MDS matrix used by current ('03) Whirlpool is also used by WHIRLBOB as a countermeasure to the structural observations given in [60]. Our design is based on Whirlpool 3.0.

Whirlpool was found to be vulnerable to a Rebound Distinguisher [35,36,39]. That 2^{188} attack applies to the 10-round variant; our 12-round version should offer a comfortable security margin, especially as our security target is 2^{192}. The way the round constants are derived from the S-Box allows this change to be made in a straightforward manner.

5.3 Notes on the origins of Streebog, Kuznyechik, and STRIBOBr1

The 8-bit S-Box used by STRIBOBr1 was directly lifted from Streebog so that hardware and software components developed for Streebog could be shared or recycled when implementing STRIBOBr1. The same S-Box is also used by the recently proposed Russian Encryption Standard "Kuznyechik" [25,61].

The GOST R 34.11-2012 "Streebog" standard text [26] does not describe the linear step as a 8×8 matrix-vector multiplication with $\mathsf{GF}(2^8)$ elements like the STRIBOBr1 spec [56], but as a 64×64 binary matrix multiplication. One can see that $8 \times 8 \times 8 = 512$ bits are required to describe the former, but $64 \times 64 = 4096$ bits are required for the latter. The more effective description was discovered by Kazymorov and Kazymorova in [33] by exhaustively testing all 30 irreducible polynomial bases, revealing an AES-like MDS structure. The origin of the particular numerical values of that MDS matrix is still a mystery. They do not appear to offer similar avenues for size or performance optimization like those in Whirlpool 3.0 and STRIBOBr2 do.

Not much about the particular design criteria of the Streebog S-Box has been published. That S-Box was apparently selected at least 5 years ago as Streebog already appeared in RusCrypto '10 proceedings [38]. Very recent ongoing work has revealed it to also have an optimized representation [16], after all.

We can easily observe that the S-box offers reasonable resistance against basic methods of cryptanalysis. Its differential bound [13] is $P = \frac{8}{256}$ and best linear approximation [37] holds with $P = \frac{28}{128}$. There does not seem to be any exploitable algebraic weaknesses. These are the exact same bounds as can be found for the Whirlpool and STRIBOBr2 S-Box, but fall short from the bounds of the AES S-Box.

By comparison, the Rijndael AES S-Box is constructed from finite field inversion x^{-1} operation in $\mathsf{GF}(2^8)$ (inspired by the Nyberg construction [49]) and an affine bit transform that serves as a countermeasure against, among other things, Interpolation Attacks [31] on the AES predecessor SHARK [52]. We refer to [23] for more information about the AES design process.

We had brief informal discussions with some members of the Streebog and Kuznyechik design team at the CTCrypt '14 workshop (05-06 June 2014, Moscow RU). Their recollection was that the aim was to choose a "randomized" S-Box that meets the basic

differential, linear, and algebraic requirements. Randomization using various building blocks was simply iterated until a "good enough" permutation was found. This was seen as an effective countermeasure against yet-unknown attacks. At the time of Streebog S-Box selection (before 2010's) the emergence of allegedly effective AES Algebraic Attacks such as [22] was a major concern for much of the symmetric cryptographic community. Hence it was felt appropriate to avoid too much algebraic structure in either the S-Box or MDS matrix while also ensuring necessary resistance against known attacks such as DC and LC. Algebraic attack attempts of this type against AES have since largely fizzled out. We feel confident that the Whirlpool S-Box should be sufficient for our claimed security level, especially as it offers significantly better speeds in constant-time implementations when compared to an AES-Style S-Box.

One is left with the impression that Streebog is a "whitened" or randomized copy of the original Whirlpool design. Despite its partially unknown origins and relative shortcomings on some implementation targets, we consider STRIBOBr1 to be at least as secure as STRIBOBr2 if appropriately implemented. Indeed some of the more successful attacks on AES adn Whirlpool have been based on their deep structural self-similarities and simplistic key schedules [14,15,17], so STRIBOBr1 may have some security advantages against "unknown" attacks.

6 Conclusions

We have introduced WHIRLBOB, an algorithm for Authenticated encryption with Associated Data. WHIRLBOB is a variant of the STRIBOBr1 first round CAESAR candidate but borrows its main components from the Whirlpool 3.0 hash. WHIRLBOB, also known as STRIBOBr2, is a CAESAR [21] second round candidate [58].

WHIRLBOB has extremely small implementation footprint on resource-limited software platforms – typically under half a kilobyte. Its particular S-Box and MDS design allows WHIRLBOB to have efficient constant-time bitsliced and SIMD byte shuffling implementations. This is an effective countermeasure against cache timing attacks, which are a concern against AES. The $b = 8 \times 64$ - bit state size is particularly suitable for bitslicing of a byte-oriented algorithm on 64-bit platforms and byte slicing for SIMD platforms.

WHIRLBOB has superb implementation characteristics on FPGA (ASIC), SIMD and lightweight embedded platforms. We recommend WHIRLBOB especially for those platforms. Furthermore WHIRLBOB offers provable security assurance through its security relationship with the well-analyzed Whirlpool hash.

We have also discussed the design choices for the STRIBOB S-Box and other components used in the Streebog hash and Kuznyechik cipher, which are becoming standards for the Russian security market.

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A WHIRLBOB 1.0 π "8-bit" Reference Implementation

This ANSI C function implements the WHIRLBOB 512×512-bit π permutation.

```
void wbob_pi(uint8_t st[64])                // WHIRLBOB Pi
{
  int r, i, j;
  uint8_t t[64], x, *pt;

  for (r = 0; r < 12; r++) {                // 12 rounds
    for (i = 0; i < 64; i++) {
      t[(i & 7) + ((i + (i << 3)) & 070)] = // P
        wbob_sbox[st[i]];                   // S
    }

    // The round constants C come from the S-box
    pt = (uint8_t *) &wbob_sbox[8 * r];
    for (i = 0; i < 8; i++)
      st[i] = pt[i];                        // C in first 8
    for (i = 8; i < 64; i++)
      st[i] = 0;                            // zero the rest

    // Apply the circular, low weight MDS matrix
    for (i = 0; i < 64; i += 8) {
      pt = &st[i];                          // start of row
      for (j = 0; j < 8; j++) {
        x = t[i + j];                       // Circular MDS
        pt[j & 7] ^= x;                     // 01
        pt[(j + 1) & 7] ^= x;               // 01
        pt[(j + 3) & 7] ^= x;               // 01
        pt[(j + 5) & 7] ^= x;
        pt[(j + 7) & 7] ^= x;

        // x <- 02
        x = (x << 1) ^ (x & 0x80 ? 0x1D : 0x00);
        pt[(j + 6) & 7] ^= x;               // 02

        // x <- 04
        x = (x << 1) ^ (x & 0x80 ? 0x1D : 0x00);
        pt[(j + 2) & 7] ^= x;               // 04
        pt[(j + 5) & 7] ^= x;               // 01 + 04 = 05

        // x <- 08
        x = (x << 1) ^ (x & 0x80 ? 0x1D : 0x00);
        pt[(j + 4) & 7] ^= x;               // 08
        pt[(j + 7) & 7] ^= x;               // 01 + 08 = 09
      }
    }
  }
}
```